

**AMENDMENTS TO THE CLAIMS**

**Listing of claims:**

This listing of claims replaces all prior versions and listings of claims in the application.

Claims 1-5 (Canceled)

Claim 6 (Currently Amended) A method of fabricating a semiconductor device, comprising the steps of:

forming a gate oxide film on a substrate by a thermal oxide film;

forming a gate electrode pattern on said gate oxide film;

forming diffusion regions in said substrate at both lateral sides of said gate electrode pattern by introducing an impurity element into said substrate through said gate oxide film while using said gate electrode pattern as a mask; and

introducing N atoms into said gate oxide film while using said gate electrode pattern as a mask, such that said N atoms do not penetrate into the substrate, and

forming a contact hole through said gate oxide film,

said step of introducing said impurity element being conducted prior to said step of introducing N atoms into said gate oxide film,

wherein said step of introducing N atoms into said gate oxide film comprises a thermal annealing process of said gate oxide film conducted in an atmosphere containing NO,

wherein activation of said impurity element is conducted simultaneously to said thermal annealing process,

said thermal annealing process being conducted at a temperature of about 800°C over a duration of 5 minutes or more after introducing N atoms to said gate oxide film such that there occurs concentration of N atoms at an interface between said substrate and said gate oxide film,

said method further comprising the step of depositing, after said step of introducing N atoms, a CVD-oxide film on said gate oxide film by a CVD process,

wherein said step of introducing N atoms and said step of depositing said CVD-oxide film are conducted consecutively in a common processing chamber, without taking out said substrate into an atmospheric environment.

Claims 7-18 (Canceled)